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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/092,158	06/05/1998	SAILESH M. MERCHANT	MERCHANT3333	5736

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/092,158	MERCHANT ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-12 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The final rejection as set forth in paper No.24 is withdrawn in response to applicants' response.

2. A new 103(a) rejection is made as set forth in this Office Action.

3. Claims 1, 4-12 and 15-24 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5, 6, 8-12, 16, 17 and 19- 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 5,591,671) in view of Bai et al. (U.S. 5,714,418) and McTeer (U.S. 6,204,179 B1).

In reference to claims 1, 12 and 24, Kim et al. (Figs.2-4) in a related method to form an interconnect layer teach the steps of forming a contact opening (25) in a dielectric layer (24) on a semiconductor substrate (21, 24), said contact opening (25) electrically contacting an active device; depositing by physical vapor deposition (PVD) a barrier layer (26, 27) in said contact opening (25) and on at least a portion of said semiconductor substrate (21, 24), said barrier layer deposition step includes depositing titanium layer (26) and depositing titanium nitride layer (27) on said titanium layer (26); depositing a contact metal (28) on said barrier layer (26, 27) within said contact opening (25); removing a substantial portion of said contact metal (28) and said barrier layer (26,

27) from said semiconductor substrate (21, 24) to form a contact plug within said contact opening (25); and subjecting said contact plug to a temperature gradient (column 4, line 27 – column line 23).

Kim et al. fail to show extending the plug to an uppermost surface of said substrate. However, Bai et al. (Figs.4C-4D) in a related method to form interconnects in a semiconductor device teach the steps of removing a substantial portion a contact metal (44) and a barrier layer (42, 43) from a semiconductor substrate (40, 41) to form a contact plug within a contact opening (47), said plug extending to an uppermost surface of said substrate (40, 41) (column 9, lines 12-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to extend the plug to an uppermost surface of said surface as taught by Bai et al. in the interconnect forming method of Kim et al., since this would result in a planarized interconnect with reduced the contact resistance and improved performance of the circuit (column 9, lines 26-42).

Kim et al. in combination with Bai et al. fail to teach the step of subjecting said contact plug to a temperature sufficient to anneal said barrier layer. However, McTeer (Figs.6) in a related method to form interconnects teaches subjecting a contact plug (3) to a temperature sufficient to anneal a barrier layer (13, 4, 6) (column 19, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to anneal the contact plug as taught by McTeer in the combined interconnect structure of Kim et al. and Bai et al., since this would improve the contact resistance of the interconnect structure (column 19, lines 12-33) and improve the coverage of the contact plug (column 3, line 63 – column 4, line 14).

In reference to claims 5, 6, 16 and 17, Kim et al. teach depositing a tungsten contact by chemical vapor deposition (column 4, line 57 – column 5, line 4).

In reference to claims 8, 9, 19, 20 and 23, Kim et al. in combination with Bai et al. and McTeer teach depositing a barrier layer including forming a thickness of said barrier layer ranging from about 90 nm to about 290 nm within said contact opening having a design width below 1μ and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater (Kim et al., column 4, lines 38-44). Kim et al. in combination with Bai et al. and McTeer fail to teach the thickness of said barrier layer from about 5 nm to about 20 nm and having 5% to about 20% of field area thickness within said contact opening. However, the selection of the claimed ranges is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

In reference to claims 10, 11, 21 and 22, Kim et al. in combination with Bai et al. and McTeer teach removing a substantial portion including removing said contact metal and said barrier layer from said field area thickness by chemical mechanical polishing processes (Kim et al., column 5, lines 62-67 and Bai et al., lines column 9, lines 12-24).

6. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. ('671) in view of Bai et al. ('418) and McTeer ('179) as applied to claims 1, 5,

6, 8-12, 16, 17 and 19-24 above, and further in view of the applicants admitted prior art in the instant application.

Kim et al. in combination with Bai et al. and McTeer teach depositing a barrier layer in a contact opening in a dielectric layer, but fail to show the contact opening with an aspect ratio ranging from about 3:1 to about 5:1. However, the prior art teaches forming openings having aspects ratios from about 3:1 to about 5:1 (page 2, lines 1-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify aspect ratios of about 3:1 to about 5:1 as taught by the prior art and include it in the combination of Kim et al., Bai et al. and McTeer, since this fulfill the need for forming smaller devices (page 1, line14 - page 2, line 6).

7. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. ('671) in view of Bai et al. ('418) and McTeer ('179) as applied to claims 1, 5, 6, 8-12, 16, 17 and 19-24 above, and further in view of Teo (U.S. 5,970,374).

Kim et al. in combination with Bai et al. and McTeer teach subjecting said contact plug to a thermal process (Kim et al., column 5, lines 9-14) but fails to teach using a rapid thermal anneal (RTA) process. However, Teo in a related method to form interconnects teaches the step of using rapid thermal anneal at a temperature of about 670°C for about 30 seconds (column 4, lines 17-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a RTA process as taught by Teo and in the combination of Kim et al., Bai et al. and McTeer, since this improves the adhesion of the barrier layer in the contact opening (column 4, lines 17-25).

Response to Argum nts

8. Applicant's arguments filed 11/01/2002 have been fully considered but they are not persuasive.

Applicants' argue "...a person having ordinary skill in the art would not be motivated to find or add to Kim the teachings and suggestions of Bai, inasmuch as Bai does no address the problem of preventing oxidation of Kim's barrier and ohmic contact layers..". Also, applicants' argue "...one who is skilled in the art would have no motive to insert Bai's step of heat treating the barrier layers before depositing the metal because this step runs contrary to Kim's goal of preventing oxidation of the barrier layer and ohmic contact layer by depositing a refractory metal layer over the barrier and ohmic contact layers before heat treatment..." (page 3, lines 1-13). In response to this argument, Bai was not relied on upon that purpose. The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, by extending the planarized plug of Kim et al. as taught by Bai et al. to an uppermost surface of said substrate, a planarized interconnect with improved performance of the circuit would be obtained.

Conclusion

9. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

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